WHAT IS CLAIMED IS:

1. An insulat d gate field effect semiconductor d vic comprising:

a semiconductor layer including a channel region;

semiconductor source and drain regions provided within or in contact with said semiconductor layer with said channel region therebetween;

a gate electrode provided adjacent to said channel region; and

a gate insulating layer interposed between said gate electrode and said channel region,

wherein at least a portion of said semiconductor layer is doped with one or more elements selected from the group consisting of carbon, nitrogen and oxygen, said portion being a region between said channel region and source region or between said channel region and drain region.

2. The device of claim 1 wherein said source and drain regions and said channel region comprise a silicon semiconductor and said at least a portion of said semiconductor layer comprises silicon carbide, silicon nitride, silicon oxide or mixture thereof.

3. The device of claim 2 wherein said silicon carbide is Si_XC_{1-X} ($0 \leq X < 1$) and said silicon nitride is Si_3N_{4-X} ($0 \leq X < 4$) and said silicon oxide is SiO_{2-X} ($0 \leq X < 2$).

4. The device of claim 2 wherein said source and drain regions are doped with an impurity element selected from Group III and Group V of the Periodic Table.

5. The device of claim 1 wherein said portion is doped with one or more elements of carbon, nitrogen and oxygen at a

conc ntration of 1 X 10^{19} atoms·cm^{-3} or mor .

6. The method of claim 1 wherein both of the regions between the source and channel regions and between the drain and channel regions are doped with said one or more elements.

7. The device of claim 6 wherein said both of the regions extend into said channel region, respectively.

8. The device of claim 1 wherein said channel region is provided in protrusion of a semiconductor substrate.

9. The device of claim 1 wherein the source region comprises two regions different from each other in impurity concentration and the drain region comprises two regions different from each other in impurity concentration.

10. In a method for forming an insulated gate field effect semiconductor device comprising a source and a drain, a channel region extending between said source and said drain, a gate electrode located adjacent to said channel region and a gate insulating layer interposed between said gate electrode and said channel region, the improvement comprising the steps of:

forming a conductive layer on the gate insulating layer provided on a semiconductor layer;

patterning said conductive layer to make at least one opening in said conductive layer;

introducing at least one of carbon, nitrogen and oxygen into said semiconductor layer through said opening; and

forming the gate electrode by removing portions of the patterned conductive layer.

11. The method of claim 10 further comprising the step of forming a source and a drain in said semiconductor layer by implanting impurities into said semiconductor layer with said gate electrode as a part of mask.

12. The method of claim 10 wherein said introducing step is carried out by ion implantation.

13. In a method for forming an insulated gate field effect semiconductor device comprising a source and a drain, a channel region extending between said source and said drain, a gate electrode located adjacent to said channel region and a gate insulating layer interposed between said gate electrode and said channel region, the improvement comprising the steps of:

forming a mask pattern having at least one opening therein on a semiconductor film; and

introducing at least one of carbon, nitrogen and oxygen into said semiconductor film through said opening.

14. The method of claim 13 further comprising the steps of:

removing said mask pattern after said introducing step; and

forming the gate electrode on said semiconductor film with the gate insulating layer therebetween after said removing step.

15. The method of claim 14 further comprising the step of forming a source and a drain in said semiconductor film by implanting impurities into said semiconductor film with said gate electrode as a part of mask.

16. The method of claim 13 wherein said mask pattern comprises a material selected from the group consisting of a photoresist and a semiconductor and an insulating material and a metal.

17. The method of claim 13 wherein said mask pattern is formed on the gate insulating layer provided on said semiconductor film and said at least one of carbon, nitrogen and oxygen is introduced into said semiconductor film through said opening with said gate insulating layer between said semiconductor film and said mask pattern.

18. The method of claim 13 wherein said introducing step is carried out by ion implantation.

19. A method for forming an insulated gate field effect semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

forming a conductive film on said insulating film;

forming a gate electrode by removing a portion of said conductive film;

forming a source and a drain in said semiconductor substrate by introducing impurities into said semiconductor film with said gate electrode as a part of mask;

forming a source electrode and a drain electrode on said source and said drain, respectively; and

introducing at least one of carbon, nitrogen and oxygen into said semiconductor substrate with said gate electrode and said source electrode and said drain electrode as masks.

20. The method of claim 19 wherein said introducing step is carried out by ion implantation.